

“PCIe-TC BOARD STANDARD GPIO OPERATIONS”

FIELD APPLICATION NOTE

(requires board software revision “A4” or later)

Background:

This document explains how to use the General Purpose Input Output (GPIO) option for standard PCIe-TC boards, including all PCIe-LTC, PCIe-VITC, and PCIe-VLTC boards. Board software revision “A4” or later is required in all cases. The GPIO option allows a PCIe-TC board to sense up to 4 digital inputs (such as switch closures), and to drive up to 2 opto-relay outputs or 4 digital outputs.

Board Hardware Requirements:

The GPIO option for PCIe-TC boards is an option which can be added to existing boards, but you will have to return the board(s) to the factory to have the work done, update the board software if needed, get a bracket change, and get it all tested.

General Purpose Input (GPI) On-Board Hardware Description:

As stated earlier, the standard GPIO option for PCIe-TC boards includes 4 inputs. These 4 inputs are called “GPI1” through “GPI4”. Each input can be modeled as having a 33kohm pullup resistor to +3.3V (when the host PC is powered up). The input signal is RC low pass filtered, then connected to an A/D converter input. By default, an input voltage above about +2.0V is “high”, and an input voltage below about +1.2V is “low”. Hysteresis is employed to prevent signals between +1.2V and +2.0V from changing the output state. An open input will float “high” because of the pullup resistor, and a grounded input will be “low”. A TTL level digital input will have no trouble meeting the required “low” voltage, but may in some cases have trouble exceeding the “high” voltage. We recommend $V_{oh} = +2.4V$ minimum. The internal 33kohm pullup to +3.3V should help in this regard. Each input is sampled about every 1ms by the A/D converter. The on-board processor then does some digital filtering, applies hysteresis, and updates the input line status bits approximately every 16ms. Our use of an A/D converter for sampling the input lines is a bit unusual, but this allows for the sampling of other signal types on a custom order basis.

General Purpose Input (GPI) Software Interface:

The state of inputs “GPI1” through “GPI4” can be read at any time from DPRAM register 0Ah (bits not listed are reserved) (bits are updated approximately every 16ms):

- Bit 3 => GPI4 status.
- Bit 2 => GPI3 status.
- Bit 1 => GPI2 status.
- Bit 0 => GPI1 status.

General Purpose Input (GPI) Data Change Interrupts:

If desired, the on-board processor can generate an interrupt whenever any of the 4 GPI input lines changes state in DPRAM register 0Ah. This allows the host PC to concentrate on other things until a GPI data change occurs, without having to continuously poll DPRAM register 0Ah. The interrupt code for GPI data changes is 88h. This value will appear at board-to-host mailbox port 0Fh soon after each data change is detected, provided that you have enabled data change interrupts by setting bit 4 high in DPRAM register 2Eh. Be careful not to alter any other bits in DPRAM register 2Eh (interrupt enables) inadvertently. See standard board documentation for further details (if needed) about receiving interrupt codes, etc..

General Purpose Output (GPO) On-Board Hardware Description (General):

As stated earlier, the standard GPIO option for PCIe-TC boards includes up to 4 outputs. These 4 outputs are called "GPO1" through "GPO4". By default, each output is "TTL" digital logic type. On a special order basis, it is possible to have opto-relay outputs instead. The following two sections describe these two configurations in more detail.

General Purpose Output (GPO) On-Board Hardware Description (TTL Case):

By default, the standard GPIO option for PCIe-TC boards includes 4 "TTL" outputs. These are not really TTL level outputs, but rather more general purpose digital logic outputs. Each output can be modeled as having a 332ohm resistor in series with a +3.3V CMOS driver output. Thus an unloaded "high" output should be near +3.3V, and an unloaded "low" output should be near ground. In addition, each output has a heavy duty 5V Transient Voltage Suppressor (TVS) zener diode to ground, to protect the on-board drivers from ESD damage, and to reduce high frequency output noise. Output circuitry should be designed to keep GPO pin voltages between ground and +3.3V in order to avoid turning on the protection diodes in either the forward or reverse directions.

General Purpose Output (GPO) On-Board Hardware Description (Opto-Relay Case):

By special order, the GPIO option for PCIe-TC boards can include 1 or 2 "opto-relay" outputs. Each opto-relay occupies two GPO output pins, so GPO1 and GPO2 could be the two ends of one opto-relay, and GPO3 and GPO4 could be the ends of a second opto-relay. The opto-relays are designed for switching signals, not power, up to 24VAC and 200mA maximum, with an "on" resistance of 15ohms maximum. An on-board 36V bi-directional TVS device is attached between each opto-relay lead and ground, for circuit protection purposes. **DO NOT CONNECT 115VAC OR 230VAC POWER TO THE OPTO-RELAY LEADS!!!**

General Purpose Output (GPO) Software Interface:

Outputs “GPO1” through “GPO4” can be changed at any time by writing directly to DPRAM register E8h (bits not listed are reserved):

Bit 3 => GPO4 control.

Bit 2 => GPO3 control.

Bit 1 => GPO2 control.

Bit 0 => GPO1 control.

DPRAM register E8h may also be read at any time to determine the current state of the GPO output controls. By default, all GPO outputs are “high impedance” when a board first powers up or is reset. Once the values in register E8h have been initialized as desired, bit 7 of DPRAM register E9h must be set high (“1”) in order to enable all of the GPO output pins. Setting E9h bit 7 low (“0”) disables all the GPO output pins again. For the “TTL” output case, when enabled, setting a bit high (“1”) in register E8h sets the corresponding GPO output pin high, and vice-versa. For the “opto-relay” output case, the GPO1 and GPO3 control bits have no effect, the GPO2 control bit must be set LOW in order to turn on the GPO1-GPO2 relay, and the GPO4 control bit must be set LOW in order to turn on the GPO3-GPO4 relay. The relays are turned off by setting the GPO2 and/or GPO4 control bits high, or by setting E9h bit 7 low (global disable) (the default case).

Connector Pinout:

A standard 9-pin “D” connector (with pin contacts) is used for the GPIO connections. This connector attaches to a 2x5 (10-pin) header on the PCIe-TC board via a short ribbon cable. The “D” connector may be mounted directly onto a full-height PCIe-TC board bracket (this is the default case), or may be mounted onto a separate low-profile bracket. The pinout of the 9-pin “D” connector (and the 2x5 header) is as follows:

Pin 1 => GPI3

Pin 2 => GPI4

Pin 3 => GPO4

Pin 4 => GPO3

Pin 5 => GPO1

Pin 6 => GPI1

Pin 7 => GPO2

Pin 8 => GPI2

Pin 9 => Chassis Ground

Note that there should be tiny (almost invisible) pin numbers molded onto the connector face. Be careful not to be “off by one” pin number. When looking at the pin contact side of the PCIe-TC GPIO connector, pin 1 is at the left end of the top (5-pin) row, and pin 6 is at the left end of the bottom (4-pin) row.

External Cabling and EMI/RFI:

Because of the almost unlimited variety of possible applications for the PCIe-TC board's GPIO pins, we cannot tell you how to wire things up externally. We can suggest that the external signal sources and destinations use the same electrical ground that is used by the host PC (in which the PCIe-TC board is installed). This helps to avoid signal disruptions and possible circuit damage due to radio transmitters, cell phones, lightning, AC power distribution issues, and other electrical disturbances. We can also suggest that the external wiring be reasonably short (3m/10' maximum), with a grounded shield if necessary, both to minimize unwanted RF emissions (RFI) and to guard against electromagnetic interference (EMI).

Hardware/Software Testing Ideas:

During your GPIO hardware/software development, and for PCIe-TC board testing purposes, you may find it useful to conduct one or more of the following tests. For example, for the "TTL" output case, temporarily connect an LED anode to 9-D pin 5 (GPO1), and the cathode to 9-D pin 9 (ground), then verify that your software can turn the LED on and off by setting and clearing the GPO1 control bit in DPRAM register E8h. The on-board series 332ohm resistor will limit the LED current to about 7mA. If an LED is not handy or convenient, you can instead use a voltmeter or oscilloscope to verify the same thing. Be sure to set the "enable" bit in DPRAM register E9h (see documentation).

Once you are able to control output GPO1, you can temporarily connect it to GPI1, and verify that whenever your software changes the state of GPO1, there is a corresponding change (after several milliseconds delay) in the state of GPI1. This "loopback test" can also be used to trigger a GPI data change interrupt if desired (see documentation).

If an opto-relay is installed, it can be tested by tying one end to ground (9-D pin 9), tying the other end to GPI1, and verifying that whenever the relay is turned on, GPI1 gets pulled low (to ground).

Remember that all of the GPO output pins have heavy duty TVS circuit protection devices installed which are "invisible" during normal operations, but will clamp signals to ground which exceed the rated circuit voltages (board damage could occur in this case).

THAT'S ALL! Please give us a call if you need any help.